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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,970	12/11/2003	Theodore W. Houston	TI-35974	8532

23494 7590 08/17/2005

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EXAMINER	
PHAN, TRONG Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/732,970	HOUSTON, THEODORE W.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/11/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the high input/output voltage VDDI/O (lines 2-3, page 20 of the specification). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to

which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It is not understood what the high input/output voltage VDDI/O (lines 2-3, page 20 of the specification) really is since it is not shown in the drawings of the present invention.

It is not understood how the sources of all three transistors 210, 220 and 230 in Fig. 2 of the present invention are connected to both Vnwell and VDD as illustrated by only a black node. This is not described in the specification. Furthermore, as shown in Fig. 4 of the present invention, the Vnwell is provided to the back gates of the P-channel transistors of the SRAM cell, meanwhile, VDD in Fig. 2 is not seen in Fig. 4 and Vpwell OR SUBSTRATE in Fig. 4 is not seen in Fig. 2.

It is not understood how the gates of the three P-channel transistors 210, 220 and 230 are interconnected.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 2-13, 15-23 and 28-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2 and 15, it is not clear how the sleep mode voltage controller can provide the array high supply voltage VADD relative to a well voltage. What is the degree or type of relationship between the array high supply voltage VADD and the

well voltage? The word "relative" is vague and indefinite.

Claim 3, it is not clear how the sleep mode voltage controller can provide the array low supply voltage VASS relative to a substrate voltage. What is the degree or type of relationship between the array high supply voltage VADD and the substrate voltage? The word "relative" is vague and indefinite.

Claims 4 and 16, it is not understood how the sleep mode voltage controller can provide a well voltage at about the high operating voltage VDD during the sleep mode.

Claims 5-6 and 17-18, it is not clear what transistor parameters really are.

Claims 7 and 19, it is not clear how the sleep mode voltage controller can employ only a component selected from the group consisting of a transistor, a diode and a low-drop out regulator. The sleep mode voltage controller must comprise the combination of a transistor, a diode and a low-drop out regulator as shown in Fig. 2 of the present invention.

Claims 8 and 20, it is not clear what a set of optimum values for a general technology class of transistors really are.

Claims 9 and 21, it is not clear how the sleep mode voltage controller can adjust the array high supply voltage VADD and the array low supply voltage VASS based on a sleep mode current.

Claims 10 and 22, it is not clear how the sleep mode voltage controller can adjust the array high supply voltage VADD and the array low supply voltage VASS based on a diode leakage current.

Claims 11 and 23, it is not clear how the sleep mode voltage controller can provide a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are about a same voltage. Fig. 4 of the present invention shows these voltages are not the same.

Claims 12-13, it is not clear what the voltage across the SRAM array that is sufficient for data retention really is.

Claims 28-29, the word "relative" is vague and indefinite.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-29 are, insofar as understood, rejected under 35 U.S.C. 103(a) as being unpatentable over Andersen et al., 6,434,076.

Andersen et al., 6,434,076, discloses in Fig. 1 a SARM device comprising: four SRAM sub-arrays 10, 20, 30 and 40 coupled to row decoder 50 and column decoder 60;

power management circuits 91, 92, 93 and 94 each can be a new SRAM power management circuit 600 as shown in Fig. 7 which provides internal power supply voltage Vdd having a high-level of 0.6 V lower than high operating voltage Vdd of 1.2 V and a low-level of 0.3 V higher than low operating voltage ground during a

sleep mode under the control of the sleep control signal 320 as shown in Fig. 8; wherein: SRAM device is refreshed during the sleep mode (see lines 55-58, column 3 and lines 55-58, column 7).

What is not shown in Andersen et al., 6,434,076, is the features as recited in claims 2-13, 15-23 and 25-29.

However, since these features are not clearly understood as being rejected under 35 USC 112, first and second paragraphs, as set forth above, therefore, claims 2-13, 15-23 and 25-29 would also have been rendered obvious under 35 USC 103(a) as being unpatentable over Andersen et al., 6,434,076.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, HOAI HO can be reached on (571)272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRONG PHAN
PRIMARY EXAMINER

Approved
TP
8/13/05

FIG. 1

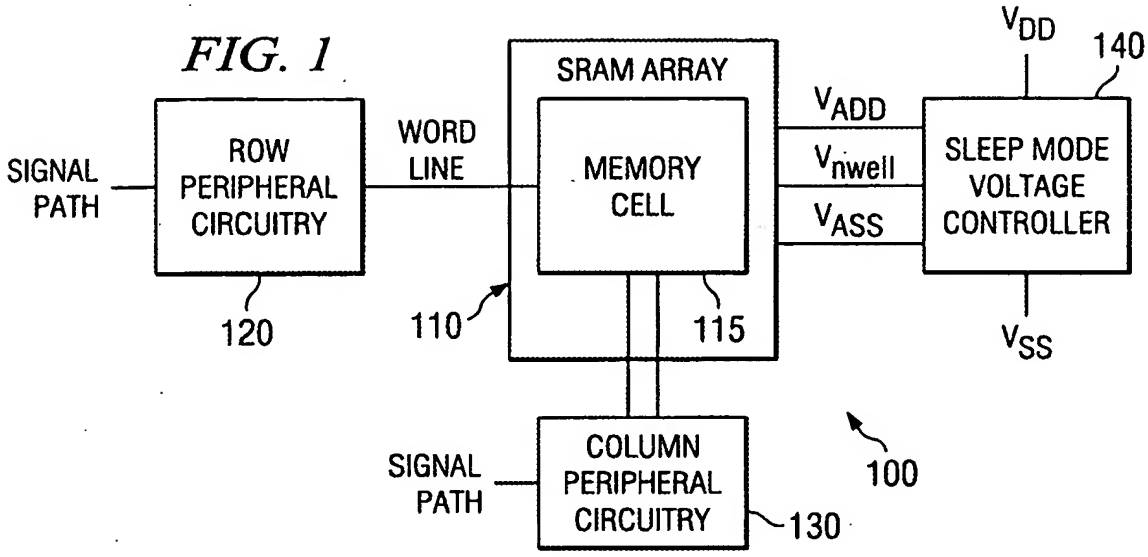
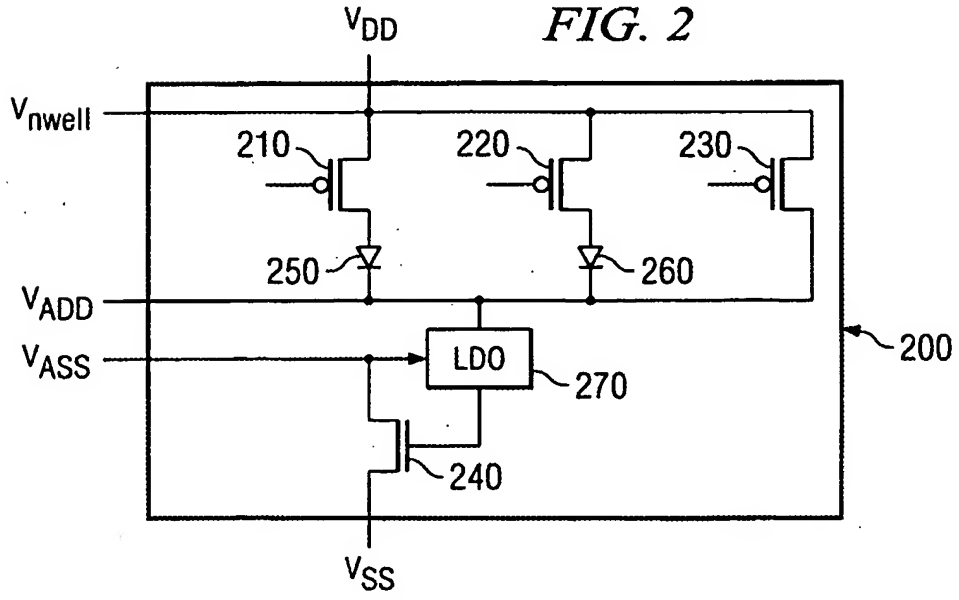


FIG. 2



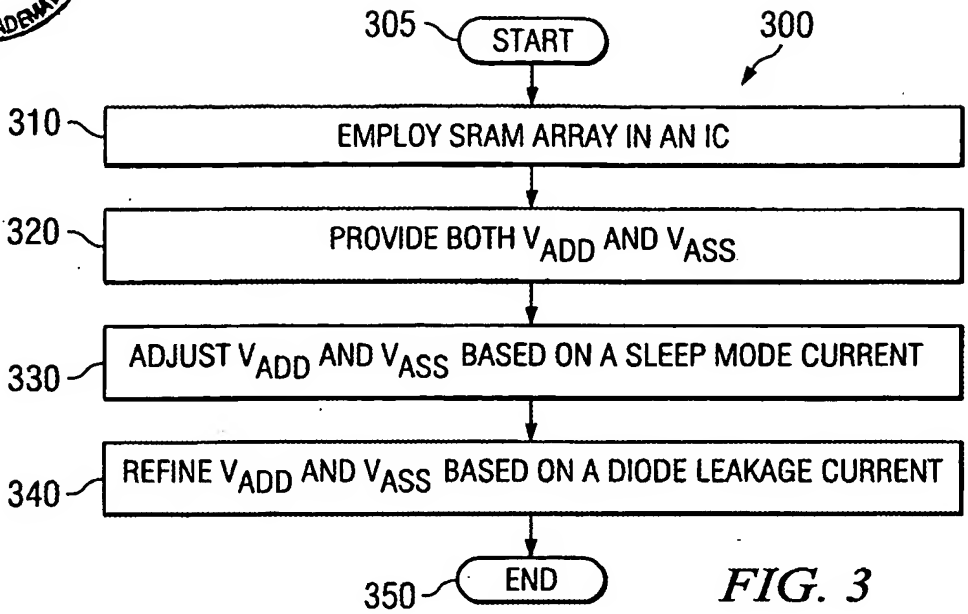


FIG. 3

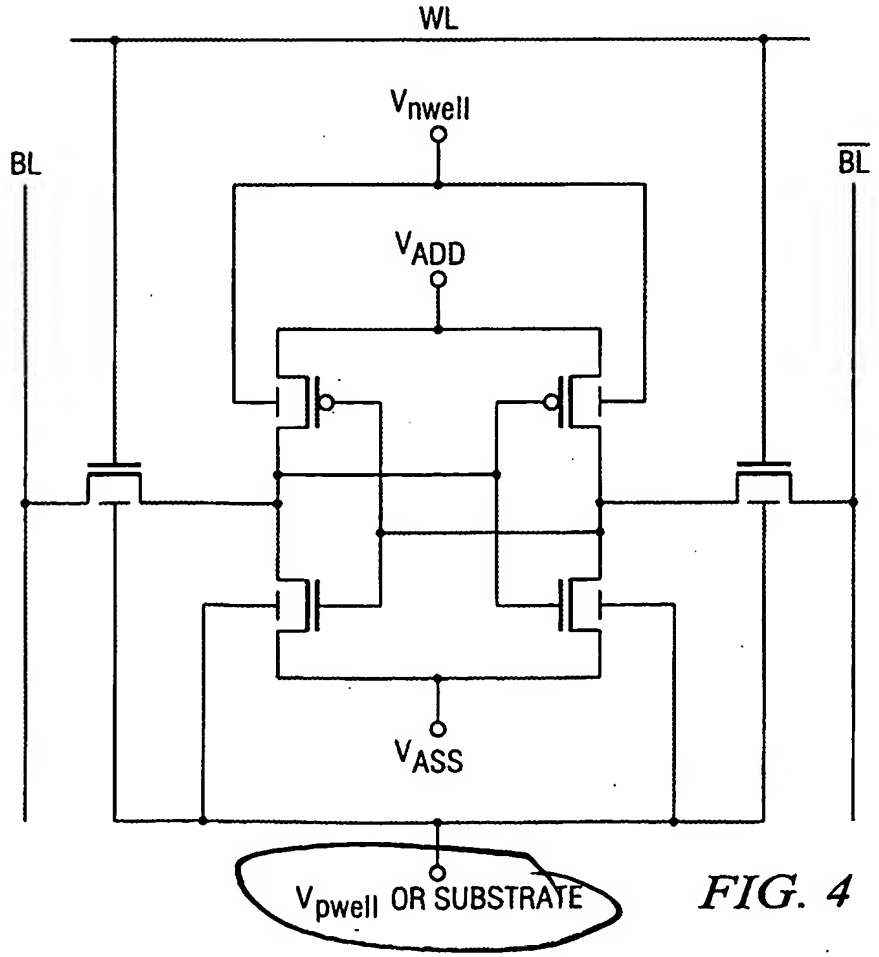


FIG. 4